AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the above-referenced application.

Listing of Claims:

1. (Currently amended) A semiconductor memory device having a memory cell array comprised of memory cells requiring refresh, in which a read request or write request is asynchronously given for an access address, wherein the semiconductor memory device comprises:

a refresh timer periodically outputting a refresh request signal for said memory cell array;

a late write writing control circuit ~~writing~~ that writes, for said write request, an access address and write data for a write request given in a memory cycle before a memory cycle for the write request by a late write operation; and

a refresh control circuit performing a refresh operation for said memory cell array in response to the refresh request signal from said refresh timer, and delaying performance of said refresh operation until a read operation or the late write operation for a memory cell for the ~~colliding~~ read request or the write request is completed when said refresh request signal collides with said read request or said write request, wherein said refresh control circuit includes circuitry that generates a control signal for said refresh operation and a control signal for said read operation or said late write operation based on (i) said refresh request signal and (ii) a delay signal responsive to the colliding of said read request or said write request with said refresh request signal.

2. (Original) The semiconductor memory device according to claim 1, wherein said refresh timer has a timer switching capability of setting a timer cycle during an active mode to be shorter than a timer cycle during a standby mode involving a refresh operation as a timer cycle in which its refresh request trigger is generated.

3. (Original) The semiconductor memory device according to claim 1, wherein said refresh control circuit comprises:

a refresh control pulse generator circuit having a capability of inputting a memory accessing enable signal, an address transition detection signal from a late write register storing memory access addresses, a refresh request trigger from said refresh timer and outputting a latch control signal controlling a latch operation of memory access addresses, a refresh address count-up signal, and a row enable normal signal and row enable refresh signal, and delaying the output of said row enable refresh signal until said latch control signal falls when the refresh request signal from said refresh timer is inputted during output of said latch control signal;

a refresh address counter inputting the refresh address count-up signal outputted from said refresh control pulse generator circuit to count up the refresh address;

a multiplexer inputting a row address (X address) of said memory access addresses and a refresh address outputted from said refresh address counter, and switch-wise outputting any one of the addresses to an X decoder as X address;

a MUX control circuit inputting the row enable normal signal and row enable refresh signal outputted from said refresh control pulse generator circuit, and outputting to said multiplexer a normal address transfer control signal and refresh address transfer

control signal controlling the switching of the X address outputted from said multiplexer; and

sense enable/precharge enable control circuit controlling a sense amp/precharge circuit of said memory by the row enable normal signal and row enable refresh signal outputted from said refresh control pulse generator circuit.

4. (Currently amended) A semiconductor memory device having a memory cell array comprised of memory cells requiring refresh, the semiconductor memory device comprising:

a refresh request generator circuit generating a refresh request independently of a read request or write request for said memory cells; and

a refresh control circuit delaying performance of ~~said~~ a refresh operation until a read operation or write operation for said memory cells for said read request or write request is completed when the refresh request from said refresh request generator circuit collides with said read request or write request, wherein said refresh control circuit includes circuitry that generates a control signal for said refresh operation and a control signal for said read operation or said write operation based on (i) said refresh request signal and (ii) a delay signal responsive to the colliding of said read request or said write request with said refresh request signal.

5. (Original) The semiconductor memory device according to claim 4, wherein the write operation of performing said write operation is a late write operation of writing an access address and write data for a write request given in a memory cycle before a memory cycle for said write request.

6. (Original) The semiconductor memory device according to claim 5, further comprising an address storing apparatus storing the present write request address, and an address hit control circuit making a comparison between the read request address and the write request address stored said address storing apparatus at the time of the previous write request, and outputting an address hit signal when the former and the latter match each other.

7. (Currently amended) [[The]] A semiconductor memory device having a memory cell array comprised of memory cells requiring refresh ~~according to claim 6~~, the semiconductor memory device comprising:

a refresh request generator circuit generating a refresh request independently of a read request or write request for said memory cells;

a refresh control circuit delaying performance of said refresh until a read operation or write operation for said memory cells for said read request or write request is completed when the refresh request from said refresh request generator circuit collides with said read request or write request; and

an address storing apparatus storing the present write request address, and an address hit control circuit making a comparison between the read request address and the write request address stored said address storing apparatus at the time of the previous write request, and outputting an address hit signal when the former and the latter match each other,

wherein the write operation of performing said write operation is a late write operation of writing an access address and write data for a write request given in a memory cycle before a memory cycle for said write request, and

wherein said semiconductor memory device has a page mode function, and is provided with said address storing apparatus and said address hit control circuit for each of a page address and an address other than said page address.

8. (Original) The semiconductor memory device according to claim 7, further comprising an address hit control circuit for page mode outputting a logical signal of an address hit signal of said page address and an address hit signal of the address other than said page address.

9. (Currently amended) [[The]] A semiconductor memory device having a memory cell array comprised of memory cells requiring refresh ~~according to claim 4~~, the semiconductor memory device comprising:

a refresh request generator circuit generating a refresh request independently of a read request or write request for said memory cells; and

a refresh control circuit delaying performance of said refresh until a read operation or write operation for said memory cells for said read request or write request is completed when the refresh request from said refresh request generator circuit collides with said read request or write request,

wherein said refresh control circuit further comprises:

a one shot pulse generator circuit generating a one shot signal having one logic level in response to an address transition;

a latch circuit holding said one logic level of said one shot pulse;

a delay circuit delaying the output of said latch circuit by a predetermined time period;

a refresh request generator circuit generating a refresh request signal in response to said refresh request;

a refresh pulse generator circuit generating a timing control signal for the refresh operation in response to the output signal of said latch circuit and said refresh request signal; and

a memory accessing pulse generator circuit generating a timing control signal for said read operation or write operation and a latch control signal based on the output signal of said latch circuit and the output signal of said delay circuit.

10. (Original) The semiconductor memory device according to claim 9, wherein said predetermined time period is set based on a refresh operation time period.

11. (Original) The semiconductor memory device according to claim 9, wherein said latch circuit is reset at the other logic level in response to said latch control signal.

12. (Original) The semiconductor memory device according to claim 9, wherein when the output signal of said latch circuit is at said one logic level, said refresh operation is prohibited, and said read request address or write request address is accessed.

13. (Original) The semiconductor memory device according to claim 11, wherein when the output signal of said latch circuit is at said other logic level, the refresh operation based on said refresh request is performed.

14. (Original) The semiconductor memory device according to claim 9, wherein said refresh request is generated from a refresh timer operating independently of said read request or write request.

15. (Original) The semiconductor memory device according to claim 9, further comprising other latch circuit holding said one logic level of the enable signal inputting said read request or write request; and

a logic circuit inputting the output signal of said latch circuit and the output signal of said other latch circuit,

wherein said refresh pulse generator circuit generates the timing control signal of the refresh operation in response to the output signal of said logic circuit and said refresh request signal, and

said memory accessing pulse generator circuit generates the timing control signal of said read operation or write operation and the latch control signal based on the output signal of said logic circuit and the output signal of said delay circuit.

16. (Original) The semiconductor memory device according to claim 15, wherein said other latch circuit is reset at the other logic level in response to said latch control signal.

17. (Original) The semiconductor memory device according to claim 15, wherein when any one or both of the output signal of said latch circuit and the output of said other latch circuit are at said one logic level, said refresh operation is prohibited, and said read request address or write request address is accessed.

18. (Original) The semiconductor memory device according to claim 15, wherein when both of the output signal of said latch circuit and the output signal of said other latch circuit are at said other logic level, the refresh operation based on said refresh request is performed.

Claims 19 and 20 (Cancelled).